## 25.5 A 2.2GHz Sub-Harmonic Mixer for Direct-Conversion Receivers in 0.13µm CMOS

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The direct-conversion receiver architecture permits increased integration and lower cost. However, it also presents several design challenges. Nearly all of these are related to the generation of large or time-varying dc offsets at the output of the receiver. While static offsets can be calibrated out, mechanisms that give rise to random time-varying offsets must be suppressed. The two primary sources of offsets are even-order nonlinearities and LO leakage to the RF input. This work focuses on addressing the latter using sub-harmonic mixers (SHMs) in the receiver front-end. It is noted that even with offset cancellation, a mixer with small dc offsets is desirable to reduce the dynamic range required of the succeeding amplifier/filter stage and offset cancellation circuitry. The dynamic range reduction translates to power savings. This 2.2GHz CMOS SHM achieves a dc offset of 0.7mV without calibration. At the input of the SHM, the 2×LO leakage is -91dBm, and the LO leakage is -95dBm.

Different ways exist for converting with a sub-harmonic LO. The technique used here combines two 90° phase-shifted LOs to generate a virtual LO at the RF (2×LO) frequency [1]. The SHM is implemented in 0.13µm digital CMOS technology with no analog options or thick top-metal layer. It consists of a preamplifier, a passive switching network, a polyphase filter and an LO buffer (Fig. 25.5.1). The input is matched to 100Ω differential on-chip without any external components. This is done so that the mixer can be utilized in applications where an external filter is needed between the LNA and the mixer. The output is loaded by a voltage buffer. Differential structures are used throughout the circuit. This topology demands very little headroom, and therefore is easily adaptable to future scaling. The preamplifier is an inductively degenerated common-source stage. A pseudo-differential topology is chosen over fully-differential for better linearity. Practical values of on-chip inductors necessitate the addition of a capacitor in parallel with $C_{gs}$ to assist in input matching. The low Q of these inductors limits the gain and noise performance of this stage, especially the 7nH single-ended inductor in series with the gate. Figure 25.5.3 shows the measured $S_{11}$.

The passive switching network has two parallel paths. Each is made up of two resistive ring mixers in cascade. First consider the path on the top in Fig. 25.5.1. If the two cascaded ring mixers are driven by two 90° phase-shifted square-wave LOs with a 50% duty cycle, and the switches are assumed to be ideal, then the transfer function through the path is equivalent to that of a single ring mixer driven by a 2×LO square wave. Sub-harmonic mixing action is attained. The conversion loss is theoretically π/2 or 4dB. Figure 25.5.2 illustrates this principle in the frequency domain. Essentially the two mixers in cascade are "correlated." The first square wave spreads the signal at 2×LO onto the odd harmonics of the second square wave. Then the second square wave converts these sidebands down to dc. Note that no filtering should be added in between the two mixers in an attempt to remove these sidebands. Also the image of the first mixer is at dc. So the preamplifier must either have an inductive load to shunt low-frequency noise at its output, or be ac coupled to the switching network.

The $C_{gs}$ of a MOS transistor changes with bias conditions. So the coupling from LO1+ and LO1- onto the switching network input nodes (nodes S+ and S- in Fig. 25.5.1) is imbalanced during the crossover, causing a 2×LO signal on these nodes. This happens even in a perfectly matched ring mixer. To further suppress 2×LO leakage, the bottom path is introduced in parallel. This path is identical to the top one except that the LOs are applied in the reverse order. Now the signal on these nodes is at 4×LO, outside the passband of the preamplifier. A post-layout simulation of the LO coupling onto node S+ is shown in Fig. 25.5.3 for one period of the LO. The addition of the bottom path also ensures that the switching network maintains a more constant load on the preamplifier while switching. Figure 25.5.4 shows the measured 2×LO and LO leakage at the SHM input.

Since the preamplifier is ac coupled to the passive switching network, no direct current flows in the switches, even if the switches and bias resistors are mismatched. There are no static offsets due to device mismatch. DC offsets are measured with the RF port terminated. Hence all offsets at the output are caused by LO self-mixing. Figure 25.5.4 shows the measured dc offsets at the SHM output.

In this design, the output of the mixer is loaded by a high impedance, which avoids the magnification of the succeeding amplifier's noise as occurs in a current-mode passive mixer [2]. The pole at the output sets the IF bandwidth to 7MHz. Figure 25.5.5 shows the measured conversion gain and DSB noise figure. At 1MHz IF, the gain is 4.5dB and the noise figure is 11dB. Although 1/*f* noise in passive mixers has been measured and reported [2], in general, CMOS passive mixers still have better 1/*f* noise performance than their active counterparts [3, 4]. The measured 1/*f* corner of this mixer is 100kHz. It is not as low as that of the passive fundamental mixers described in [3, 4], but it is still comparable to that of a well designed active CMOS mixer without noise cancellation.

The external LO is passed through a two-stage polyphase filter to generate the necessary phases and then converted to full-rail square waves to drive the switching network. The required LO input power is -18dBm. The measured IIP2 and IIP3 of the SHM are +35dBm and 0dBm, respectively (Fig. 25.5.6). The preamplifier consumes 7.2mW while the LO buffer consumes 5.5mW from a 1.2V supply. Figure 25.5.7 shows a die micrograph.

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*References:*
[1] K. Lee, et al., "A Single-Chip 2.4-GHz Direct-Conversion CMOS Receiver for Wireless Local Loop using Multiphase Reduced Frequency Conversion Technique," *IEEE J. Solid-State Circuits*, vol. 36, pp. 800–809, May, 2001.
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[3] E. Sacchi, et al., "A 15 mW, 70 KHz 1/f Corner Direct Conversion CMOS Receiver," *Proc. IEEE CICC*, pp. 459–462, Sept., 2003.
[4] S. Zhou, M.C. Chang, "A CMOS Passive Mixer With Low Flicker Noise for Low-Power Direct-Conversion Receiver," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1084–1093, May, 2005.

 

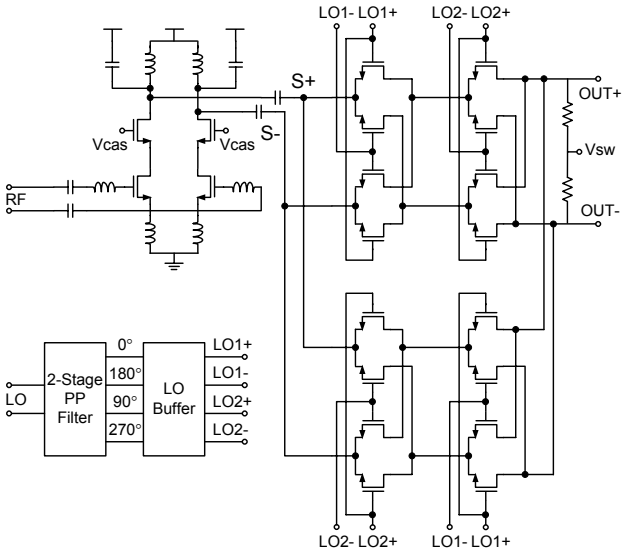


Figure 25.5.1: Schematic of the sub-harmonic mixer.

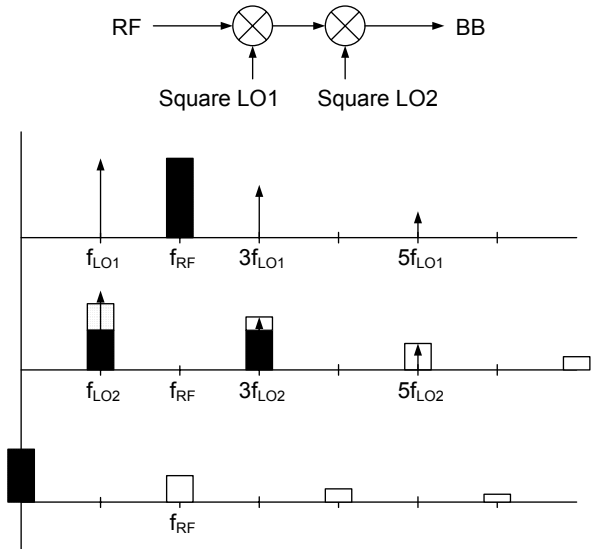


Figure 25.5.2: Sub-harmonic mixing action in the frequency domain.

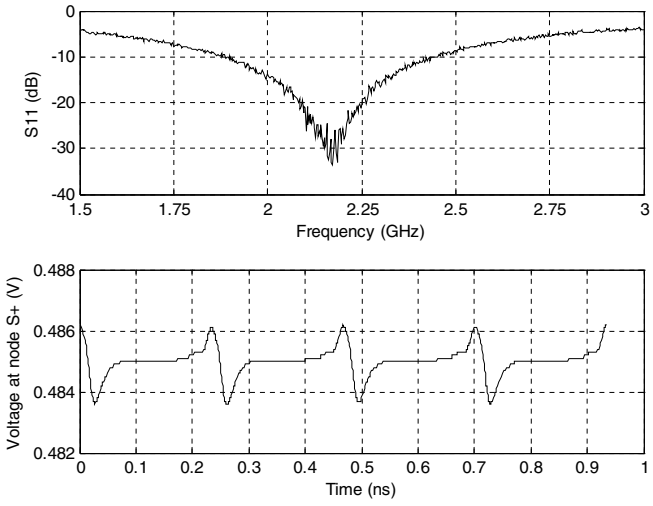


Figure 25.5.3: $S_{11}$ of the SHM (top) and LO coupling onto node S+ in Fig. 25.5.1 (bottom).

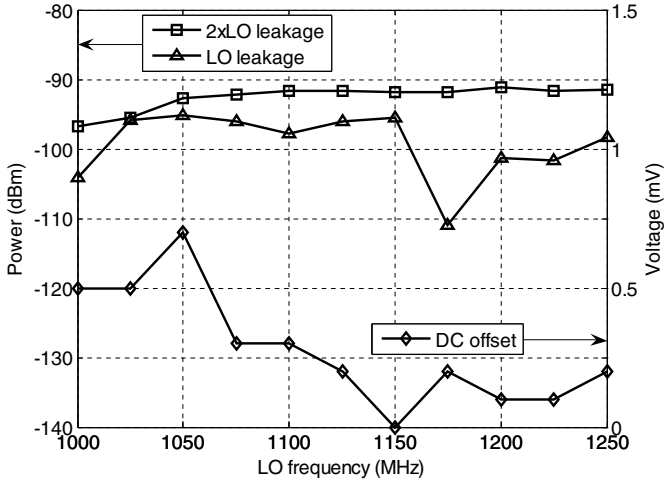


Figure 25.5.4: LO leakage at the RF port and dc offset at the SHM output.

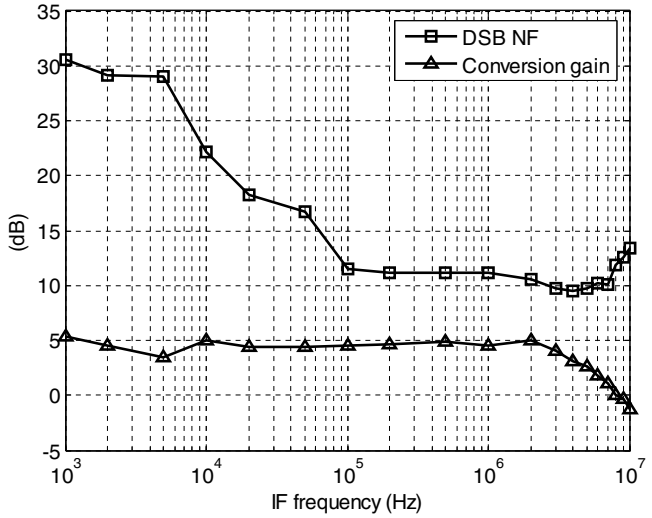


Figure 25.5.5: Measured noise figure and conversion gain.

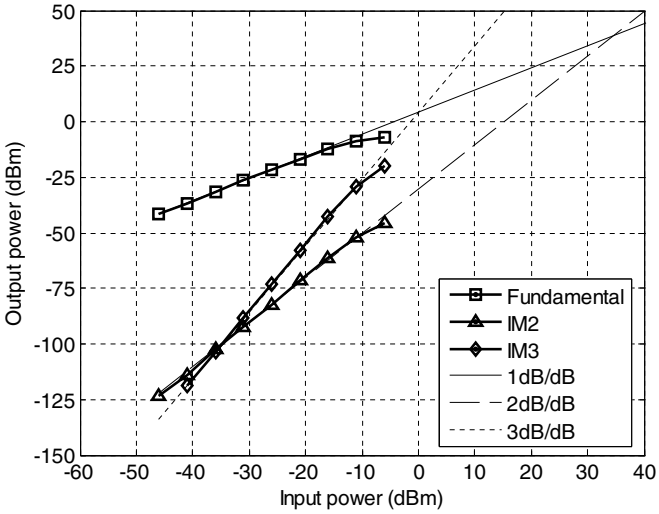


Figure 25.5.6: Linearity characteristics of the SHM.

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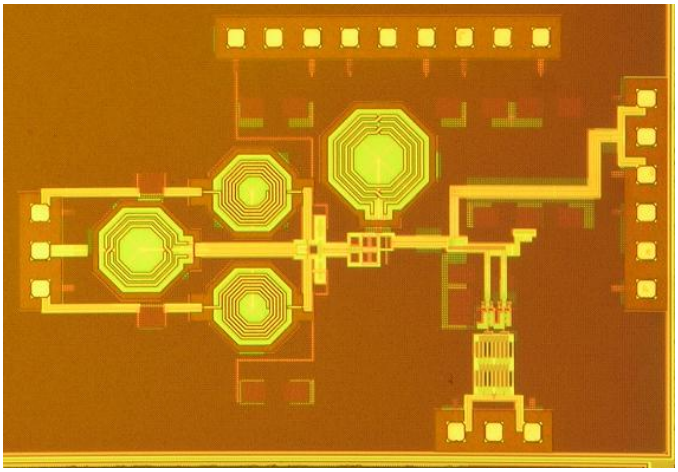

Figure 25.5.7: Die micrograph.

 